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09/889,260	01/03/2002	Siegfried Hart	83256	1457

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Welsh & Katz  
22nd Floor  
120 South Riverside Plaza  
Chicago, IL 60606-3913

EXAMINER

NGUYEN, MINH T

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 05/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/889,260

Applicant(s)

HART ET AL.

Examiner

Minh Nguyen

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*h*

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 March 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 5 and 6 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 5 and 6 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 July 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

1. Applicants' amendment filed 3/24/03 has been received and entered in the case. Claims 5-6 are pending. The objections to the drawings are remained because no response is seen in the amendment. New grounds of rejections necessitated by the amendment are set forth below. This action is FINAL.

#### ***Drawings***

2. The drawings are objected to because the block circuits 1-9 shown in Fig. 1 and the block circuits 1-2 and 4 shown in Fig. 5 do not have text labels. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

#### ***Specification***

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because:

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- (i) it is not in the range of 50 to 150 words,
- (ii) it is not sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

Correction is required. See MPEP § 608.01(b).

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Low Jitter Analog-Digital Phase Locked Loop with Lock Detection Circuit".

#### ***Claim Objections***

5. Claim 5 is objected to because of the following informalities:

lines 1-2, "a high-frequency output clock signal" should be changed to -- an output clock signal -- to be consistent with the terms used on lines 6, 10 ..., to avoid potential antecedent basis problem,

lines 6 and 10, the terms "the oscillator" should be changed to -- the digitally controllable oscillator --,

line 19, "look detection circuit" should be changed to -- lock detection circuit --.

Appropriate correction is required.

#### ***Claim Rejections - 35 USC § 112***

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

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The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 5, the claim is indefinite because it fails to particularly point out the structural relationships between elements. The recited relationships between the digitally controllable oscillator, drive circuit, digital phase detector, analog phase detector and lock detection circuit are unclear and confusing. The recitation that the drive circuit sets the output clock signal until the phase error which is specified by a counter reading is zero appears incorrect because as described in the specification, the counter 3 is merely a divider, and as shown in Fig. 1 of the present invention, the driver 8 does not detect whether the counter reading of the divider 3 is zero or not as recited. The recitation that the digital phase detector compares the signals via a PI filter and the drive circuit is confusing, i.e., as shown in Fig. 1, the digital phase detector 1 compares the reference signal REF\_CLK and the signal output from the counter 3, not via the PI filter and the drive circuit as recited. The recitation that the lock detection circuit activates the digital phase detector if the phase exceeds a specific phase error on the last paragraph appears misdiscriptive because as shown in Fig. 1, the lock detection circuit does not have any structure to control the digital phase detector, i.e., the communication between the digital phase detector 1 and the lock detection circuit 4 is a one way communication, and because of this structure, the lock detection circuit 4 cannot activate the digital phase detector as recited.

As per claim 6, this claim is indefinite because of the indefiniteness of claim 5.

***Claim Rejections - 35 USC § 102***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 5-6 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No.

6,028,460, issued to McCollum et al.

As per claim 5, McCollum disclose an electronic phase-locked loop (Fig. 3) for the jitter-attenuated generation of an output clock signal (at the output of the VCO 240) which is phase-synchronous with respect to a reference clock signal (at the output of the oscillator 100), having:

a digitally controllable oscillator (VCO 240, the VCO 240 is seen as digitally controllable oscillator because it can be controlled by the digital PLL circuit 300),

a drive circuit (AV 330),

which digitally sets the output clock signal of the oscillator until a phase error between the output clock signal and a reference clock signal, which is specified discreetly by a counter reading of a counter, is zero (the drive circuit AV 330 sets the output clock signal generated by the VCO 240 until the reading of the divider 340 is zero, i.e., *see Fig. 1 of the present invention for the similar structure, the drive circuit 8 sets the output clock signal generated by the VCO 9 until the reading of the divider 3 is zero*),

a digital phase detector (320, it is seen as digital because it is in the digital PLL loop),

which compares the output clock signal of the oscillator (240) with the reference clock signal via a PI filter (230) and the drive circuit (as shown, the signals to the digital phase detector 320, which represent the recited signals, are compared and the result at the output of the digital phase detector 320 indicates the phase difference between these signals),

an analog phase detector (220, it is seen as analog because it is in the analog PLL loop),

a lock detection circuit (the circuit block 400) for avoiding a phase quantization error (by controlling the switch 600 to switch the loop from DLL to PLL or from PLL to DLL), and activating the analog phase detector if the phase error specified by the counter reading is zero, the activated analog phase detector regulating the, output clock signal of the oscillator in a continuously variable manner (since the phase lock loop 200 is analog, i.e., operate in a continuous manner) until the clock signal edge of the output clock signal and of the reference clock signal are fully synchronous (this is merely the function of the phase lock loop),

the lock detection circuit (the circuit block 400 controls the switch 600 to the lower position, i.e., connect the DLL to the loop and disconnect the PLL from the loop) deactivating the analog phase detector and activating the digital phase detector (using the switch 600) if the phase error between the output clock signal and the reference clock signal exceeds a specific phase error.

As per claim 6, the claim appears to read over the prior art of record, however, due to the unclear structural relationship between recited elements, patentability of the claim cannot be positively determined at this time. For now, it is assumed that the recited limitation read on the PI filter shown in Fig. 4 wherein the integral regulation reads on the circuit 435, the linear regulation reads on the circuit 460 and the addition and amplifier stage reads on the circuit 440.

***Response to Arguments***

8. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.



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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

A handwritten signature in black ink, appearing to read 'Minh Nguyen', with a long horizontal stroke extending to the right.

Minh Nguyen  
Primary Examiner  
Art Unit 2816

MN  
May 26, 2003